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1. (original) A receiver, in a digital transmission system, comprising a channel decoder for protecting a transmitted signal against channel transmission errors, the channel decoder comprising:

- a set of co-processors including at least 3 clusters of programmable co-processors for executing the functions of a digital front-end block (DFE), a channel correction block (CIN) and a forward error correction block (FEC), respectively,
- a general purpose processor (DSP) for managing control, synchronization and configuration of the channel decoder, and
- a memory (SM) shared between the clusters and the general purpose processor.

2. (original) A receiver as claimed in claim 1, wherein the set of co-processors comprises:

- a digital front-end processor (DFE) for computing:
  - base-band demodulation of the received signal,
  - a programmable Nyquist filter,

and for controlling an automatic gain control loop (AGC) and synchronization loops for time and carrier recovery,

- a fast Fourier transform processor (FFT) for performing demodulation in the case of multi-carrier systems and frequency domain equalization in the case of mono-carrier systems,
- an adaptive filter array processor (AFA) for time domain equalization, interference rejection and frequency interpolation in the case of COFDM modulation,

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- a forward error correction processor (FEC) for decoding Reed-Solomon and convolutional codes which were used during transmission.

3. (original) A broadcasting system comprising a receiver and a transmitter, in a digital video transmission system, wherein the receiver is according to any one of claim 1.

4. (original) In a digital video receiver, a method of channel decoding for protecting a transmitted signal against transmission errors, the method comprising the steps of base-band demodulation, channel correction and forward error correction of the received signal, each step being performed by a cluster of programmable co-processors, a general purpose processor with a shared memory being provided for managing control, synchronization and configuration of said clusters of co-processors.

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5. (currently amended) A computer program product for a receiver ~~computing~~ comprising a set of instructions which, when loaded into the receiver, causes the receiver to carry out the method as claimed in claim 4.

6. (currently amended) A signal for carrying a computer program, the computer program being arranged to cause a programmable device to carry out ~~the following~~ steps comprising : base-band demodulation, channel correction and forward error correction of a received digital video signal, ~~each step being performed by~~ the programmable device comprising a cluster of programmable co-processors for performing each step, and a general purpose processor with a

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shared memory ~~being provided~~ for managing control, synchronization and configuration of said clusters of co-processors.

7. (new) The receiver of claim 1, wherein the clusters of co-processors are programmable to allow for handling a plurality of data formats, and each respective cluster performs only a single one of the recited three functions.

8. (new) The method of claim 4, wherein the clusters of co-processors are programmable to allow for handling a plurality of data formats, and each respective cluster performs only a single one of the recited three steps.

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9. (new) The computer program of claim 5, wherein the clusters of co-processors are programmable for handling a plurality of data formats, and each respective cluster performs only a single one of the recited three steps.

10. (new) The signal of claim 6, wherein the clusters of co-processors are programmable for handling a plurality of data formats, and each respective cluster performs only a single one of the recited three steps.

11. (new) A channel decoder for digital video data comprising:

- an input for receiving signals in differing formats;

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- at least one first cluster comprising at least one first programmable co-processor for executing functions of a digital front-end block (DFE), which first cluster is programmable to adapt to all of the differing formats;
- at least one a second cluster comprising at least one second programmable co-processor for executing functions of a channel correction block (CHN), which second cluster is programmable to adapt to all of the differing formats;
- at least one a third cluster comprising at least one third programmable co-processor for executing functions of a forward error correction block (FEC), which third cluster is programmable to adapt to all of the differing formats;
- a general purpose processor (DSP) for managing control, synchronization and configuration of the channel cluster; and
- a memory (SM) shared between the processors.

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13. (new) The decoder of claim 12, wherein at least one of the processors is implemented in hardware.

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14. (new) The decoder of claim 12, wherein at least one of the processors is implemented in software.

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15. (new) The decoder of claim 12, wherein the decoder is adapted to receive a signal carrying a computer program for programming the processors.

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16. (new) The decoder of claim 12, wherein at least one of the first, second and third programmable co-processors comprises a cluster of co-processors.

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